

<b>L Number</b>	<b>Hits</b>	<b>Search Text</b>	<b>DB</b>	<b>Time stamp</b>
<b>1</b>	<b>224177</b>	<b>softwar</b>	<b>USPAT; US-PGPUB; EP ; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:48</b>
<b>2</b>	<b>204630</b>	<b>hardware</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:48</b>
<b>3</b>	<b>249</b>	<b>DLAT</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:48</b>
<b>4</b>	<b>2787</b>	<b>TLB</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:48</b>
<b>5</b>	<b>777140</b>	<b>target address</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:48</b>
<b>6</b>	<b>397761</b>	<b>host instruction</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:48</b>
<b>7</b>	<b>24325</b>	<b>emulat\$4</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:51</b>
<b>8</b>	<b>86440</b>	<b>software and hardware</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:51</b>
<b>9</b>	<b>51</b>	<b>(software and hardware) and DLAT</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:51</b>
<b>10</b>	<b>14</b>	<b>((s ftware and hardware) and DLAT) and TLB</b>	<b>USPAT; US-PGPUB; EP ; JP ; DERWENT; IBM TDB</b>	<b>2002/01/10 19:52</b>

<b>11</b>	<b>14</b>	<b>((s ftware and hardware) and DLAT) and TLB) and (target address)</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:52</b>
<b>12</b>	<b>12</b>	<b>(((((software and hardware) and DLAT) and TLB) and (target address)) and (host instruction)</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:52</b>
<b>13</b>	<b>3</b>	<b>(((((software and hardware) and DLAT) and TLB) and (target address)) and (host instruction)) and emulat\$4</b>	<b>USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB</b>	<b>2002/01/10 19:52</b>

=> d his

(FILE 'HOME' ENTERED AT 19:38:52 ON 10 JAN 2002)

FILE 'USPATFULL' ENTERED AT 19:40:01 ON 10 JAN 2002

L1 45 S TLB#/TI  
L2 54 S HOST INSTRUCTION  
L3 140 S DLAT  
L4 2485 S TARGET ADDRESS  
L5 15858 S EMULAT?

=> s l1 and l3

L6 1 L1 AND L3

=> s l1 and l4

L7 5 L1 AND L4

=> dis l- pn,ti

YOU HAVE REQUESTED DATA FROM 5 ANSWERS - CONTINUE? Y/(N):y

L7 ANSWER 1 OF 5 USPATFULL  
PI US 6266752 B1 20010724  
TI Reverse **TLB** for providing branch **target**  
**address** in a microprocessor having a physically-tagged cache

L7 ANSWER 2 OF 5 USPATFULL  
PI US 6208543 B1 20010327  
TI Translation lookaside buffer (**TLB**) including fast hit signal  
generation circuitry

L7 ANSWER 3 OF 5 USPATFULL  
PI US 6079003 20000620  
TI Reverse **TLB** for providing branch **target**  
**address** in a microprocessor having a physically-tagged cache

L7 ANSWER 4 OF 5 USPATFULL  
PI US 5930832 19990727  
TI Apparatus to guarantee **TLB** inclusion for store operations

L7 ANSWER 5 OF 5 USPATFULL  
PI US 5805490 19980908  
TI Associative memory circuit and **TLB** circuit